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All-Amorphous-Oxide Transparent, Flexible Thin-Film Transistors. Efficacy of Bilayer Gate Dielectrics

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Abstract: Optically transparent and mechanically flexible thin-film transistors (TF-TFTs) composed exclusively of amorphous metal oxide films are fabricated on plastic substrates by combining an amorphous Ta_2O_5/SiO_x bilayer transparent oxide insulator (TOI) gate dielectric with an amorphous zinc−indium−tin oxide (a-ZITO) transparent oxide semiconductor (TOS) channel and a-ZITO transparent oxide conductor (TOC) electrodes. The bilayer gate dielectric is fabricated by the post-cross-linking of vapor-deposited hexachlorodisiloxane-derived films to form thin SiO_x layers (v-SiO_x) on amorphous Ta_2O_5 (a-Ta_2O_5) films grown by ion-assisted deposition at room temperature. The a-Ta_2O_5/v-SiO_x bilayer TOI dielectric integrates the large capacitance of the high dielectric constant a-Ta_2O_5 layer with the excellent dielectric/semiconductor interfacial compatibility of the v-SiO_x layer in a-ZITO TOS-based TF-TFTs. These all-amorphous-oxide TF-TFTs, having a channel length and width of 100 and 2000 μm, respectively, perform far better than a-Ta_2O_5-only devices and exhibit saturation-regime field-effect mobilities of ~20 $cm^2/V\cdot s$, on-currents $>10^{-4}$ A, and current on−off ratios $>10^5$. These TFTs operate at low voltages (~4.0 V) and exhibit good visible-region optical transparency and excellent mechanical flexibility.

Introduction

The adaptation of transistors, the fundamental building blocks of modern electronics, to unconventional applications such as large-area sensors, display drivers, and radio frequency identification tags has been the focus of intensive research over the past decade.[1] Among the new materials that have recently attracted interest as active channels in unconventional transistors are transparent oxide semiconductors (TOSs), which can exhibit high carrier mobility and optical transparency, and which have received attention since the first demonstration of a transparent thin-film transistor (TFT) using a high-temperature-annealed polycrystalline ZnO semiconductor in 2003.[2] Compared to their crystalline counterparts, amorphous TOSs (a-TOSs) offer distinctive attractions such as typically lower processing temperatures, smoother surfaces, better film uniformity, and enhanced mechanical flexibility, while maintaining comparable or greater carrier mobilities.[3] The latter characteristic is largely due to the non-negligible spatial overlap of the isotropic metal s states which form the conduction band minima (CBM) and serve as the charge carrier pathways.[3a,4] This combination of characteristics positions a-TOSs as ideal candidates to use as TFT channel materials for realizing flexible, transparent electronics. Fifth period cations such as In^{3+} and Sn^{4+}, which have $[Kr](4d)^{10}(5s)^0$ electronic configurations, are ideal a-TOS candidates due to the substantial s orbital overlap, which is primarily determined by the principal quantum number (n), assuming that crystallization is suppressed. Moreover, the incorporation of aliovalent cations

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of differing size frequently stabilizes amorphous oxide phases;[5] hence, the incorporation of some smaller cations is desirable. Note that a well-dispersed CBM also exists in fourth period ZnO due to the small intercation distances.[6] Thus, films of the quaternary a-TOS, amorphous zinc−indium−tin oxide (a-ZITO), can be readily grown by sputtering or inkjet printing and afford acceptable TFT performance.[7] More intriguingly, *both* a-ZITO TOS and transparent oxide conductor (TOC) films with the same metal ion composition can be deposited by pulsed-laser deposition (PLD) at room temperature by maintaining the O_2 deposition pressure (P_{oxygen}) at a higher or a lower value, respectively.[8] While the a-ZITO TOS can serve as an efficient TFT channel material, the a-ZITO TOC is an ideal choice to serve as transparent source/drain electrodes and to ensure Ohmic contacts to the a-ZITO TOS channel.[9] Moreover, this same material can serve as the transparent gate electrode as well.

The gate dielectric is another key element in TFT devices. SiO_2, either grown thermally (when Si wafers are used as substrates) or by plasma-enhanced chemical vapor deposition (PECVD), has traditionally been used because of its ready availability, large band gap (∼9.0 eV), high breakdown strength (10−15 MV/cm), and high-quality interface with Si.[10] However, its low dielectric constant ($\kappa \approx 3.9$), together with increasing gate tunneling leakage current with decreasing thickness, introduces significant limits on circuit densities for devices using SiO_2 as the dielectric.[11] The high deposition temperature (>250 °C) further limits its application in flexible electronics, where plastic substrates are desired and low fabrication temperatures (<150 °C) are therefore required. To realize transparent, flexible (TF)-TFTs, it is therefore necessary to develop and integrate high-κ dielectrics that can be deposited at low temperature and maintain good electrical properties. Among the transparent oxide insulators (TOIs) which are potential candidates, such as Y_2O_3, ZrO_2, Ta_2O_5, HfO_2, and TiO_2, Ta_2O_5 has received much attention because of its high κ and acceptable dielectric breakdown strength.[12] There are a variety of ways to fabricate Ta_2O_5 films, which include both chemical and physical vapor deposition methods, such as ion beam sputtering, magnetron sputtering, evaporation, anodization, thermal oxidation, sol−gel techniques, atomic layer deposition, etc.[13] Since grain boundaries may act as the preferential pathways for impurity diffusion and leakage current in crystalline dielectrics, an amorphous structure is ideal, which typically also offers a smoother surface, and thus superior dielectric−semiconductor interfacial properties.[12,14]

In spite of the aforementioned attractions of these amorphous materials, TFTs exclusively composed of amorphous oxides have rarely been reported. In this contribution, we report on the first demonstration of all-amorphous-oxide TF-TFTs. While amorphous Ta_2O_5 (a-Ta_2O_5) films grown by ion-assisted deposition (IAD) at room temperature exhibit a high κ of ∼22.1, we show here that the dielectric−semiconductor interfacial properties can be greatly enhanced by introducing a thin "capping" layer (v-SiO_x) via post-cross-linking of a vapor-deposited hexachlorodisiloxane ($Cl_3SiOSiCl_3$)-derived film. Combining these a-Ta_2O_5/v-SiO_x bilayer TOI dielectrics with an a-ZITO TOS channel and a-ZITO TOC electrodes yields high-performance all-amorphous-oxide TF-TFTs on a variety of substrates, including polyethylene terephthalate (PET). These TF-TFTs exhibit acceptable optical transparency, excellent mechanical flexibility, and significantly enhanced transistor performance versus conventional rigid, opaque Si/SiO_2-based devices.

Experimental Section

Film Deposition. a-ZITO TOC electrodes of ∼100 nm thickness and a-ZITO TOS channels of ∼60 nm thickness were deposited by PLD from a hot-pressed ceramic target ($Zn_{0.33}In_{1.40}Sn_{0.27}O_3$, 25 mm diameter) at room temperature and with $P_{oxygen} = 7.0 \times 10^{-3}$ and 2.2×10^{-2} Torr, respectively. A 248 nm KrF excimer laser with a 20 ns pulse duration, operating at a power of 200 mJ/pulse and 2 Hz repetition rate, was focused onto a 1 mm × 2 mm spot size. The target was rotated at ∼5 rpm to avoid localized heating, and the target−substrate separation was maintained at 8 cm. As bottom gate electrodes for the TF-TFTs, a-ZITO TOC films (∼100 nm thick, sheet resistance: 60−65 Ω/□) were deposited on PET substrates (∼220 μm thick; Kimoto Tech. Inc.). Next, a-Ta_2O_5 TOI films of ∼70 nm thickness were deposited on both solvent-cleaned p^+-Si (Montco Silicon Tech. Inc.) and the aforementioned PET/a-ZITO TOC substrates using a custom horizontal dual-gun (HDG) IAD system (Ion Tech Inc.) equipped with two 6 cm Kaufman ion sources to generate O_2 and/or Ar ion beams. The deposition was carried out at room temperature using a 5 in. diameter Ta_2O_5 target (99.99%, Williams Advanced Materials Inc.). While the primary 1000 eV Ar ion beam sputters the target, the assisting 200 eV O_2: Ar (1:1) ion beam is directed onto the substrates at a 30° angle both before the growth process to clean the substrate surface and *in situ* during growth to tune the film properties. The substrates were continuously rotated at 15 rpm. During this process, the growth rate and ambient pressure were ∼0.28 Å/s and 4.3×10^{-4} Torr, respectively. In parallel, the a-Ta_2O_5 films were also deposited on single-crystal NaCl and Corning 1737F glass substrates for structural and optical property analyses. A v-SiO_x layer of ∼5 nm thickness was next deposited by post-cross-linking a vapor-deposited hexachlorodisiloxane (96%, Aldrich) film as previously described.[15] For capacitance and leakage current characterization, ∼50 nm thick Au electrodes were deposited by thermal evaporation at $\sim 2.0 \times 10^{-6}$ Torr, using shadow masks to define the 200 μm × 200 μm electrodes. The deposition rate was 0.02 Å/s for the first 10 nm and 0.3 Å/s up to 50 nm. For the TFT fabrication, including the Si/SiO_2-based control devices using p^+-Si/300 nm SiO_2 substrates (Montco Silicon Tech. Inc.), ∼60 nm thick a-ZITO TOS was deposited as the channel layer. Either 50 nm Au or 100 nm a-ZITO TOC top-contact source/drain electrodes were then deposited by thermal evaporation and PLD, respectively, using shadow masks

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to yield channel dimensions of 100 μm (L) $\times$ 2000 μm (W). The large W/L ratio was chosen to ensure negligible fringing electric field effects on TFT performance metric accuracy.[16]

Film and Device Characterization. Film thicknesses were measured with a Veeco Dektak 150 surface profiler. X-ray diffraction (XRD) $\theta-2\theta$ scans were performed on a Rigaku DMAX-A instrument using Ni-filtered Cu Kα radiation. Selected area electron diffraction (SAED) patterns were obtained using a JEOL 2100 transmission electron microscope (TEM) equipped with an X-ray energy-dispersive spectroscopy system. Optical transmittance spectra were recorded using a Cary 500 UV−vis−NIR spectrophotometer. X-ray photoelectron spectroscopic (XPS) data were collected under high vacuum ($<10^{-8}$ Torr) using an Omicron ESCA probe equipped with a monochromatic Al Kα (1486.8 eV) 300 W X-ray source and an EA125 energy analyzer. The photoelectron takeoff angle was fixed at 15° to probe only atoms nearest the surface (∼1−2 nm), and the binding energies are referenced to the C 1s peak set at 284.7 eV. Atomic force microscopic (AFM) images were acquired on a JEOL-5200 scanning probe microscope in the tapping mode using silicon cantilevers (Applied NanoStructures Inc.). Capacitance versus frequency measurements were acquired by impedance spectroscopy (IS) using a Hewlett-Packard 4192A impedance analyzer. Direct current (dc) metal−insulator−semiconductor (MIS) and TFT measurements were performed on a Signatone probe station with a Keithley 6430 sub-femtoamp remote source meter and a Keithley 2400 source meter using locally written Labview software. All electric measurements were carried out in air at room temperature with no intentional blocking of light.

Results and Discussion

This section first describes the growth of a-Ta_2O_5 films by IAD at room temperature, as well as the analysis of their microstructural, optical, compositional, morphological, and dielectric properties by XRD, SAED, UV−vis−NIR, XPS, AFM, IS, and leakage versus voltage measurements. While IAD-derived a-Ta_2O_5 films exhibit high κ and large C_i with smooth surfaces and good optical transmittance, introducing a ∼5 nm v-SiO_x "capping" layer yields a-Ta_2O_5/v-SiO_x bilayer dielectrics with excellent insulating properties. It is then shown that, in the field-effect performance of a-ZITO TOS-based TFTs, the thin v-SiO_x layer enhances the dielectric−semiconductor interfacial compatibility, suppresses hysteresis, and affords superior TFT performance versus a-Ta_2O_5 dielectric devices. The novel concept of all-amorphous-oxide TF-TFTs composed *exclusively* of amorphous transparent oxide materials, including the a-Ta_2O_5/v-SiO_x bilayer TOI dielectric, an a-ZITO TOS channel, and a-ZITO TOC gate and source/drain electrodes, is next presented and TFT performance analyzed. The very good visible transparency and excellent field-effect performance, even after multiple bending cycles, demonstrate the attractions of all-amorphous-oxide TF-TFTs.

IAD-Derived a-Ta_2O_5 Films. IAD[17] is a scalable vapor-phase technique for large-area film growth, utilizing two ion beams simultaneously to optimize film growth. By controlling the ion beam energy, ion current density, and the O_2 and Ar flow rates of both the primary and assisting beams, dense oxide films with controllable and reproducible electrical and microstructural properties can be grown by IAD at room temperature. A typical XRD $\theta-2\theta$ scan of a 70 nm a-Ta_2O_5 film grown on glass by IAD at room temperature is shown in Figure 1. It can be seen that the present IAD-derived Ta_2O_5 films are essentially amorphous—not unexpected for the low growth tempeartures.[13b,18] The SAED pattern (inset) also confirms the amorphous microstructure of the IAD-derived Ta_2O_5 films.

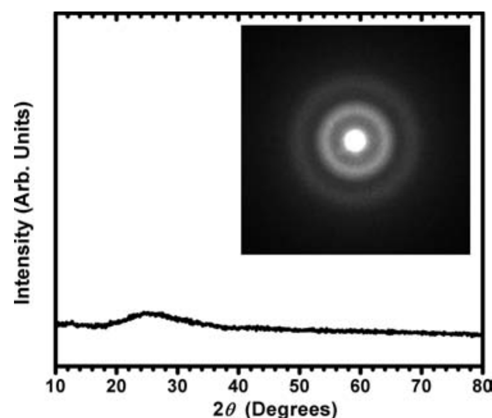

Figure 1. XRD $\theta-2\theta$ scan of an IAD-derived 70 nm thick a-Ta_2O_5 film grown at room temperature on a Corning 1737F glass substrate. The inset shows a typical SAED pattern for the a-Ta_2O_5 film.

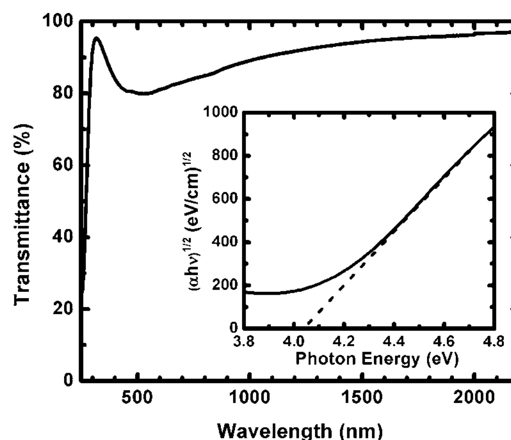

Figure 2. Optical transmittance spectrum of a 70 nm thick a-Ta_2O_5 film on Corning 1737F glass using the same glass as the reference. The inset shows the $(\alpha h\nu)^{1/2}$ versus photon energy plot of the a-Ta_2O_5 film, with the dashed line illustrating the extrapolation of the linear part to extract the E_g.

Figure 2 shows the optical transmittance spectrum of a 70 nm IAD-derived a-Ta_2O_5 film on glass. The transmittance in the visible range (400−700 nm) is >80%. The optical spectrum of the a-Ta_2O_5 film was fitted using the Tauc formalism[19] to estimate the band gap (E_g). Here the wavelength dependence of absorption coefficient (α) is described by eq 1, where B is a constant, h is Plank's constant, ν is the light frequency, and r = 1/2, 3/2, 2, or 3, depending on the electronic transition mode.

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$$\alpha = \frac{B(h\nu - E_g)^r}{h\nu} \quad (1)$$

A direct band-to-band transition has been reported for crystalline Ta_2O_5,[20] for which a linear $(\alpha h\nu)^2$ versus photon energy ($h\nu$) dependence should be observed. However, since momentum ($\hbar k$) is not conserved in an amorphous material, $r = 2$ should be used to determine the E_g for the present a-Ta_2O_5 films.[21] A plot of $(\alpha h\nu)^{1/2}$ versus $h\nu$ is shown as an inset in Figure 2. The linear dependence of $(\alpha h\nu)^{1/2}$ on $h\nu$ is obvious, consistent with the amorphous nature of the present IAD-derived Ta_2O_5 films. Extrapolating the linear portion of the plot yields $E_g \approx 4.05$ eV, which agrees well with the previously reported values for a-Ta_2O_5 in the range 4.0−4.7 eV.[22]

The a-Ta_2O_5 film composition was further analyzed using XPS. As can be seen in Figure 3a, the films exhibit a phase-pure Ta_2O_5 spectrum with negligible metal contamination. The feature at 284.7 eV is assigned to C 1s photoelectrons due to surface contamination arising from sample exposure to the atmosphere before the XPS measurement, and the peak at 530.6 eV corresponds to the metal oxide O 1s. Ta $4f_{7/2}$ and $4f_{5/2}$ binding energies are observed at 26.3 and 28.2 eV (Figure 3, top inset), respectively. These values are not unexpectedly higher than those of Ta metal and are similar to those reported for stoichiometric Ta_2O_5.[23] Note that there is only one binding state present for Ta, since only one symmetric peak with no splitting or broadening is evident for each state. The Ta features are thus attributable to Ta^{5+}. The Ta:O ratio is (0.397 ± 0.016):1, as calculated from the ratio of the corresponding integrated peaks with normalization to the atomic sensitivity factors,[23a] and further confirms the stoichiometry of the IAD-derived a-Ta_2O_5 films.

The a-Ta_2O_5 films morphologies were characterized by tapping-mode AFM. The AFM image of an a-Ta_2O_5 film grown on a p^+-Si substrate is shown in Figure 4a. The low root-mean-square (rms) roughness of ~0.17 nm indicates an extremely smooth a-Ta_2O_5 surface, which is typical of amorphous oxide films. Such an ultrasmooth surface should be beneficial to TFT device performance by reducing carrier scattering at the dielectric−semiconductor interface.[12]

The dielectric properties of the IAD-derived a-Ta_2O_5 films were investigated by measuring the frequency dependence of the areal capacitance (C_i). The results for 70 nm a-Ta_2O_5 films, grown on both p^+-Si and PET/a-ZITO TOC substrates, are shown in Figure 5a.[24] The difference between the capacitances of the p^+-Si/a-Ta_2O_5 and the PET/a-ZITO TOC/a-Ta_2O_5 samples (~250 versus ~280 nF/cm^2 at 10 kHz) doubtless reflects the thin native SiO_2 layer at the p^+-Si surface which acts as a parallel plate capacitor connected with the a-Ta_2O_5 layer in series. The

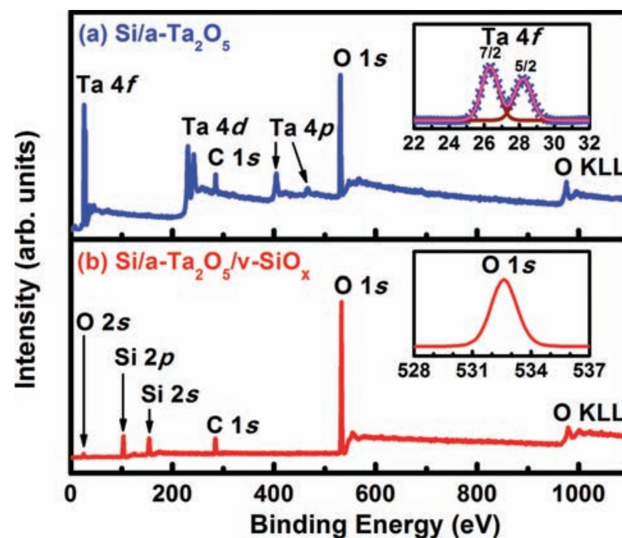

Figure 3. XPS survey spectra of p^+-Si/a-Ta_2O_5 films before (a) and after (b) v-SiO_x deposition. The top and bottom insets show the narrow scan spectra of the Ta 4f region for the p^+-Si/a-Ta_2O_5 and the O 1s region for the p^+-Si/a-Ta_2O_5/v-SiO_x samples, respectively. Curve-fitting results for the Ta 4f spectra are also shown as the brown (peaks) and pink (sum) curves, with the XPS data as blue ×'s in the top inset.

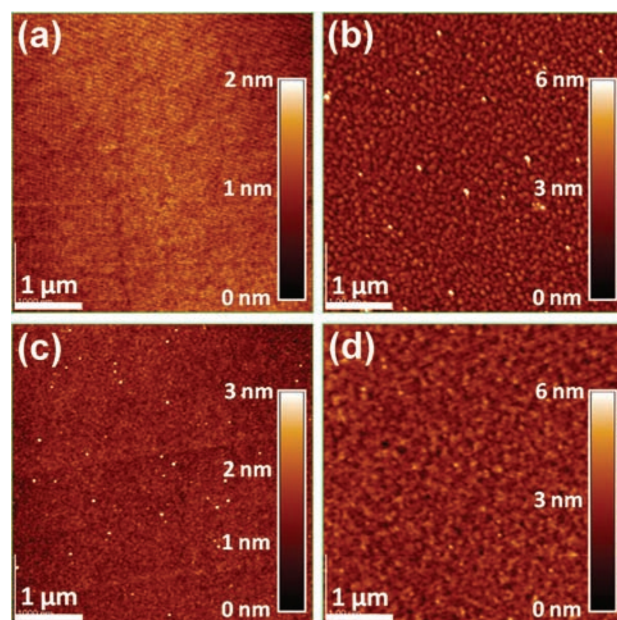

Figure 4. AFM images (4.5 μm × 4.5 μm) of p^+-Si/a-Ta_2O_5 (a), p^+-Si/a-Ta_2O_5/v-SiO_x (b), p^+-Si/a-Ta_2O_5/a-ZITO TOS (c), and p^+-Si/a-Ta_2O_5/v-SiO_x/a-ZITO TOS (d), having rms roughnesses of 0.17, 0.64, 0.22, and 0.47 nm, respectively.

dielectric constant (κ) of the a-Ta_2O_5 films is calculated from the PET/a-ZITO TOC sample data using eq 2, where ϵ_0 is the vacuum dielectric constant ($\epsilon_0 = 8.85 \times 10^{-12}$ F/m) and d is the film thickness.

$$C_i = \frac{C}{A} = \frac{\kappa\varepsilon_0}{d} \quad (2)$$

The value obtained, $\kappa = 22.1$, is in agreement with that reported for a-Ta_2O_5 films grown by other methods.[13] The native SiO_2 thickness on the p^+-Si substrate surface is estimated to be ~1.5 nm using the parallel plate capacitor equation for two capacitors in series ($1/C_{tot} = 1/C_1 + 1/C_2$).

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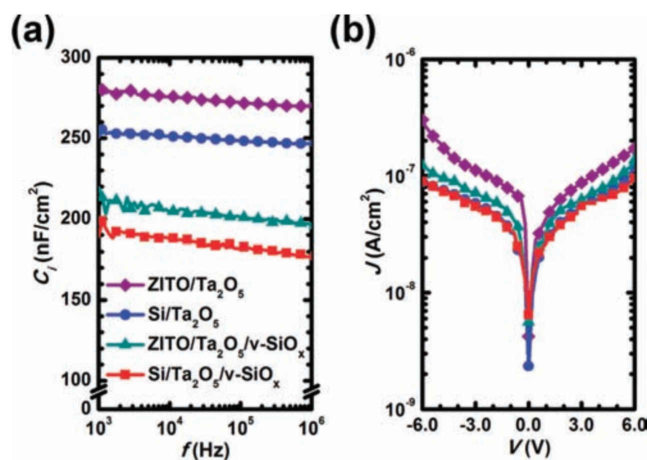

Figure 5. Capacitance versus frequency (a) and gate leakage current density versus voltage plots (b) at the voltage step of 0.2 V and the time delay of 0.1 s for 70 nm thick a-Ta_2O_5 films deposited on p^+-Si (denoted by Si in the figure legend) and PET/a-ZITO TOC (denoted by ZITO in the figure legend) substrates with and without a v-SiO_x overlayer.

The conduction mechanisms operative in Ta_2O_5 films, like many other high-κ oxide dielectrics, are complex, and a number of mechanisms have been identified, among which Schottky emission and Poole–Frenkel effects appear to dominate.[13,25] Both steady-state and transient conduction mechanisms have been identified for Ta_2O_5 films grown by various methods.[26] Transient conductivity, also known as dielectric relaxation and either Curie–von Schweidler or Kohlraush behavior, is a typical feature of disordered or amorphous dielectric films such as Ta_2O_5, which has been extensively investigated. It usually exhibits a power-law current relaxation and results in a dependence of dc leakage characteristics on gate voltage scan rate,[27] in agreement with our observation for the present a-Ta_2O_5 films on both p^+-Si and PET/a-ZITO TOC substrates (Figure S1a–d, Supporting Information). Note here that the gate leakage current density magnitude increases with gate voltage scan rate. Higher gate leakage current densities are observed at either larger voltage steps or shorter delay times. The results at the voltage step of 0.2 V and the time delay of 0.1 s are compared in Figure 5b. Note that the p^+-Si/a-Ta_2O_5 sample exhibits gate leakage current densities as low as $\sim 1 \times 10^{-7}$ A/cm^2 at ± 6.0 V. The slightly higher leakage current density in the PET/ZITO TOC/a-Ta_2O_5 sample may be related to the relatively small a-Ta_2O_5 E_g (Figure 2), and thus insufficient band offset with the a-ZITO gate electrode,[28] whereas the relatively lower leakage current density in the p^+-Si/a-Ta_2O_5 sample is likely due to the native oxide on the p^+-Si substrate. In any case, it will be seen that these artifacts are substantially reduced and transistor performance greatly enhanced by introducing a thin v-SiO_x capping layer.

a-Ta_2O_5 Films with v-SiO_x Capping Layers. Stacked high-κ Ta_2O_5/large-E_g SiO_2 multilayers have previously been fabricated by the combination of thermal growth and metal–organic chemical vapor deposition at high processing temperatures of 400–850 °C. Although such high deposition temperatures are incompatible with plastic substrates, this strategy is effective in limiting gate leakage and improving the Si/Ta_2O_5 interfacial compatibility in metal oxide–Si FETs.[29] Recent organic TFT research in this laboratory showed that SiO_x films can be grown in a low-temperature process involving post-cross-linking of a vapor-deposited hexachlorodisiloxane-derived film, "v-SiO_x".[15] The thin v-SiO_x layer acts as an efficient tunneling barrier, remarkably suppressing the leakage current of self-assembled high-κ organic gate dielectrics, and exhibits excellent interfacial compatibility with various organic semiconductors.[1d,15,30] In the present work, the properties of a-Ta_2O_5/v-SiO_x bilayer TOI dielectrics, prepared by depositing ~5 nm v-SiO_x using this low-temperature process on the IAD-derived a-Ta_2O_5 films, are investigated. It is seen that v-SiO_x greatly enhances dielectric–semiconductor compatibility and improves TFT performance.

The XPS spectrum of an a-Ta_2O_5/v-SiO_x bilayer is shown in Figure 3b. The features at 103.3 and 154.2 eV correspond to Si 2p and 2s photoelectrons, respectively. They are both shifted >4.0 eV from the standard values for metallic Si (99.2 and 149.8 eV)[23a] and are thus assigned to SiO_2. No Cl signal is detected, suggesting complete $Cl_3SiOSiCl_3$ hydrolysis by ambient H_2O to form the v-SiO_x layer via the aforementioned cross-linking and annealing procedure. Note that no Ta signal is detectable, which confirms complete coverage of the a-Ta_2O_5 layer. This complete coverage is also demonstrated by the existence of only one symmetric O 1s peak (Figure 3, bottom inset) observed at 532.6 eV, significantly shifted from the binding energy of 530.6 eV observed for the p^+-Si/a-Ta_2O_5 samples. Although the sample surface becomes slightly rougher versus bare a-Ta_2O_5 after the v-SiO_x deposition, evident from AFM morphology changes (Figure 4b), it is still reasonably smooth, with an rms roughness of ~0.64 nm.

The a-Ta_2O_5/v-SiO_x bilayer dielectric exhibits C_i values of ~180 and ~200 nF/cm^2 at 10 kHz for samples fabricated on p^+-Si and PET/a-ZITO TOC substrates, respectively (Figure 5a). As shown in Figure 5b, both samples exhibit impressive gate leakage properties, with the leakage current density $\sim 1 \times 10^{-7}$ A/cm^2 at ± 6.0 V. For the samples fabricated on PET/a-ZITO TOC substrates, the a-Ta_2O_5/v-SiO_x bilayer exhibits significantly decreased leakage current compared to the a-Ta_2O_5-only sample, suggesting effective leakage suppression by the v-SiO_x capping layer.[15] While all the present Ta_2O_5-based TF-TFTs function at ~4.0 V as shown below, the leakage current densities are far less than 10^{-6} A at ± 6.0 V for the a-Ta_2O_5/v-SiO_x bilayers on both substrates, important for efficient TFT operation.

TFT Fabrication and Response. Cosubstitution of ZnO and SnO_2 in equimolar amounts for In_2O_3 effects a net isovalent substitution, significantly enhancing the solid solubility of the cosubstituted pair to 40 atom %, yielding $Zn_xIn_{2-2x}Sn_xO_3$ materials.[31] This level of Zn and Sn substitution is significantly greater than the ~6 and ~1 atom % possible for individual

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Table 1. Component Materials and Device Performance Parameters Measured in Ambient for TFTs Fabricated with 60 nm Thick a-ZITO TOS Channels

no.	gate	dielectric	d/C_i^a (nm)/(nF/cm^2)	source/drain	V_{DS} (V)	μ_{FE}^b (cm^2/V·s)	I_{on} (A)	I_{on}:I_{off}	V_T (V)	SS (V/decade)	ΔV_T (V)
1	p^+-Si	SiO_2	300/10	Au	80	8.6(0.8)	10^{-3}	10^6	30	5.7	5.0
2	p^+-Si	a-Ta_2O_5	70/250	Au	4.0	12.3(0.9)	10^{-4}	10^4	1.2	0.33	−0.66
3	p^+-Si	a-Ta_2O_5/v-SiO_x	(70 + 5)/180	Au	4.0	23.1(1.0)	10^{-4}	10^5	0.88	0.17	−0.19
4	PET/a-ZITO	a-Ta_2O_5/v-SiO_x	(70 + 5)/200	ZITO	4.0	19.4(0.9)	10^{-4}	10^5	1.2	0.26	−0.11
5[c]	PET/a-ZITO	a-Ta_2O_5/v-SiO_x	(70 + 5)/200	ZITO	4.0	17.2(1.3)	10^{-4}	10^5	1.3	0.28	−0.14

[a] d = dielectric layer thickness. [b] Average of five working devices, with the standard derivation in parentheses. [c] Device no. 4 tested after bending 20 times along a curvature parallel to the channel length at a radius of 8 mm.

substitutions of Sn and Zn, respectively.[32] In the present study, a 30 atom % cosubstitution ($x = 0.3$) level was selected to ensure both a large fraction of In replacement and a safe compositional distance from the cosubstitution solubility limit. The ZITO deposition technique, PLD, is a powerful film growth method that avoids film compositional deviation from that of the target except at very high deposition temperatures, making it ideal for complex oxide film depositions.[33] While elevated deposition temperatures (>100 °C) induce ZITO crystallinity, the PLD-derived ZITO films grown on glass substrates at room temperature are essentially amorphous, as assessed by XRD and TEM.[8]

TFT device performance is characterized by several key metrics, including the field-effect mobility (μ_{FE}), drain−source current (I_{DS}), on/off ratio (I_{on}:I_{off}), threshold voltage (V_T), subthreshold gate voltage swing (SS), and operating voltages (including both the drain−source voltage, V_{DS}, and the gate voltage referenced to the source electrode, V_G).[1] High μ_{FE} values afford high saturation currents and fast switching speeds between on/off states; high I_{on}:I_{off} and low SS indicate efficient and effective modulation of I_{DS} with V_G; V_T close to 0.0 ensures low power consumption. In the saturation regime, I_{DS} and SS can be expressed by eqs 3 and 4, respectively, where W and L are the channel width and length, respectively.

$$I_{DS} = \left(\frac{W}{2L}\right)C_i\mu_{FE}(V_G - V_T)^2 \quad (3)$$

$$SS = \frac{dV_G}{d \log I_{DS}} \quad (4)$$

To achieve excellent TFT performance, large μ_{FE}, high I_{on}:I_{off}, close-to-zero V_T, and small SS metrics, as well as low operating voltages, are desired. It can be seen in eq 3 that the same I_{DS} can be achieved at a lower voltage by utilizing a larger μ_{FE} semiconductor and/or a higher C_i gate dielectric. The large C_i values of the a-Ta_2O_5 and a-Ta_2O_5/v-SiO_x bilayer dielectrics should therefore be beneficial to achieving low operating voltages.

First, a-ZITO TOS-based TFTs were fabricated on p^+-Si substrates using either a-Ta_2O_5 or a-Ta_2O_5/v-SiO_x bilayer dielectrics, with devices fabricated on conventional p^+-Si/SiO_2 (300 nm) substrates in parallel as controls. Due to their amorphous nature, the 60 nm thick a-ZITO TOS films exhibit

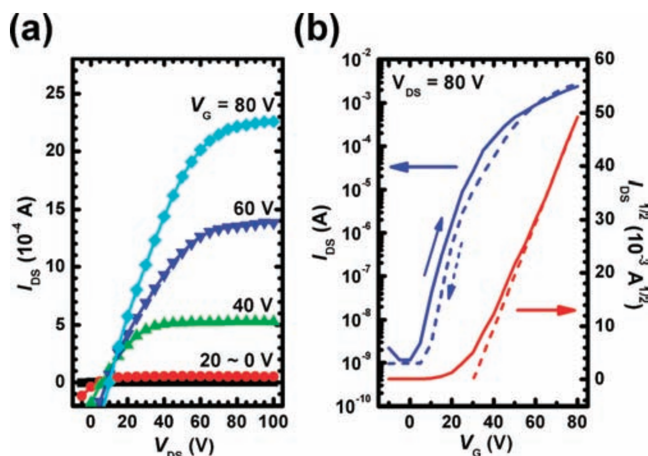

Figure 6. Representative output (a) and transfer (b) characteristics of TFTs having the structure p^+-Si/SiO_2 (300 nm)/a-ZITO TOS/Au.

almost the same surface morphologies as the substrates on which they are grown (Figure 4). The rms roughness values are a remarkable 0.22 and 0.47 nm for the samples deposited on p^+-Si/a-Ta_2O_5 and p^+-Si/a-Ta_2O_5/v-SiO_x substrates, respectively. The differences in the a-ZITO surface morphology and roughness presumably reflect the differences in substrate roughness.

The device yields are >90% for all the a-ZITO TFTs fabricated in this work. TFT characterizations were carried out in air at room temperature with no intentional light blocking, and the results are compiled in Table 1. Reported μ_{FE} values are averaged from five measurements on each type of device. Representative transfer and output characteristics are plotted in Figures 6, 7, and 9. Note that the slightly high gate leakage current (I_G, Figure S2, Supporting Information) and minor increase of I_{DS} with negative V_{DS} (Figure 7b,d) can be related to the use of unpatterned gate or semiconductor structure for these present TFTs. This is a minor effect and should decrease in well-understood ways for a gate and/or semiconductor-patterned device with much smaller gate area, hence a minimized gate leakage path.[14,34] Control TFTs using a 300 nm thick SiO_2 gate dielectric exhibit respectable performance (Figure 6). The values $\mu_{FE} \approx 9.2$ cm^2/V·s, I_{on}:$I_{off} \approx 10^6$, operating voltage of 80 V, $V_T \approx 30$ V, and SS ≈ 5.7 V/decade are all comparable to previous results.[8] The slight clockwise hysteresis with V_G shift of ∼5.0 V is likely related to the charge traps at the SiO_2/a-ZITO TOS interface.[35]

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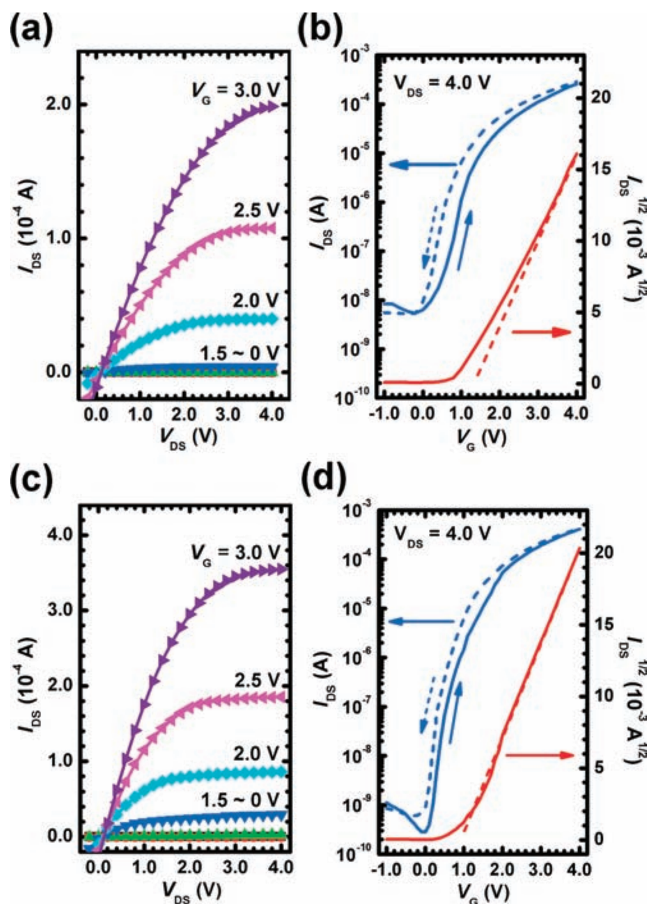

Figure 7. Representative output (a,c) and transfer (b,d) characteristics of a-ZITO TOS-based TFTs fabricated on p^+-Si substrates using either a-Ta_2O_5 (a,b) or a-Ta_2O_5/v-SiO_x bilayer (c,d) gate dielectrics.

Figure 7a,b shows representative output and transfer characteristics of the a-ZITO TOS-based TFTs fabricated on p^+-Si substrates using ~70 nm thick a-Ta_2O_5 gate dielectrics. Benefitting from the high κ and thus the large C_i of the a-Ta_2O_5 dielectric, the TFTs exhibit a significantly lower operating voltage of ~4.0 V and a SS value of ~0.33 V/decade versus the aforementioned ~80 V and ~5.7 V/decade for the SiO_2 dielectric devices. Despite the relatively high V_T (~1.2 V), a typical μ_{FE} of ~13 $cm^2/V \cdot s$, slightly higher than that of the SiO_2 devices, is obtained due to the large C_i provided by the high-κ dielectric. In contrast to the SiO_2 devices, the a-Ta_2O_5 TFTs exhibit a counterclockwise hysteresis with a negative V_G shift. There are several possible reasons for this not unusual type of TFT hysteresis: (1) charge traps at the dielectric−semiconductor interface; (2) slow polarization of the gate dielectric; and (3) charge injection, movement, and storage in the dielectric.[36] The hysteresis direction and magnitude can, in principle, be affected by all three mechanisms and determined by the dominant one. The observed counterclockwise hysteresis in these a-Ta_2O_5 devices cannot be dominated by the interface charge traps, which should result in a positive V_G shift as observed in the SiO_2 devices. Slow polarization should lead to a higher back-scan current and is usually observed in dielectrics containing polar groups that slowly move/reorient in external fields, such as in polymers having polar side groups;[37] it seems unlikely here. The present hysteresis is therefore reasonably attributable to mobile charge carriers and/or charge injection and storage in the a-Ta_2O_5 dielectric, for which there is precedent.[38]

Importantly, compared to the above a-Ta_2O_5-only results, introducing the thin, large-E_g v-SiO_x layer significantly enhances TFT performance. As extracted from the transfer plot of Figure 7d, a larger μ_{FE} of ~24 $cm^2/V \cdot s$ is achieved at ~4.0 V operating voltage for the a-Ta_2O_5/v-SiO_x bilayer TFTs. Furthermore, the a-Ta_2O_5/v-SiO_x bilayer TFTs also exhibit lower V_T (0.88 versus 1.2 V) and smaller SS values (0.17 versus 0.33 V/decade) versus the a-Ta_2O_5-only device. I_{on} reaches 0.1 mA at an operating voltage of ~2.0 V, while it requires ~2.5 V and >20 V to achieve the same current for the a-Ta_2O_5-only and commercial SiO_2 devices, respectively. These enhancements in performance metrics suggest superior v-SiO_x/a-ZITO TOS interfacial properties versus those of a-Ta_2O_5/a-ZITO TOS. Not only do the a-Ta_2O_5/v-SiO_x bilayer TFTs afford higher I_{on} values than do the a-Ta_2O_5-only devices at the same V_G, but the I_{off} (defined as the lowest observed I_{DS}) also decreases to ~10^{-9} A, comparable to typical I_{off} values of conventional p^+-Si/SiO_2-based electronics (Figure 6). In principle, charges may accumulate at the a-Ta_2O_5/v-SiO_x interface due to the conductivity differences in the a-Ta_2O_5 and the v-SiO_x layers, which will also affect the electric field distribution in each layer.[39] Nevertheless, the electric field in the a-Ta_2O_5 layer under the same applied voltage should approximately decrease on introducing the v-SiO_x capping layer according to eq 5, where E_{TaO}, t_{TaO}, E_{SiO}, and t_{SiO} are the electric field and thickness of the a-Ta_2O_5 and v-SiO_x layers, respectively.

$$E_{TaO} = \frac{V_G - E_{SiO}t_{SiO}}{t_{TaO}} \qquad (5)$$

The significantly decreased hysteresis may reflect reduced effects on the channel charge carriers of mobile ions and/or charges injected from the gate and trapped in the a-Ta_2O_5 layer because of the decreased E_{TaO} and the v-SiO_x spacer. As summarized in Table 1, the a-Ta_2O_5/v-SiO_x bilayer devices exhibit TFT performance metrics that are in every way superior to those of the a-Ta_2O_5-only devices.

All-Amorphous-Oxide TF-TFTs. The first report of a transparent TFT fabricated using a crystalline ZnO TOS channel on glass highlighted both the attractions of and fabrication challenges for such devices.[2a] A subsequent TF-TFT using an amorphous IGZO channel and polycrystalline ITO electrodes underscored these attractions and constraints.[3a] Although it is generally known that amorphous materials have greater mechanical flexibility than their crystalline/polycrystalline counterparts,[3] TF-TFTs composed *exclusively* of amorphous oxides

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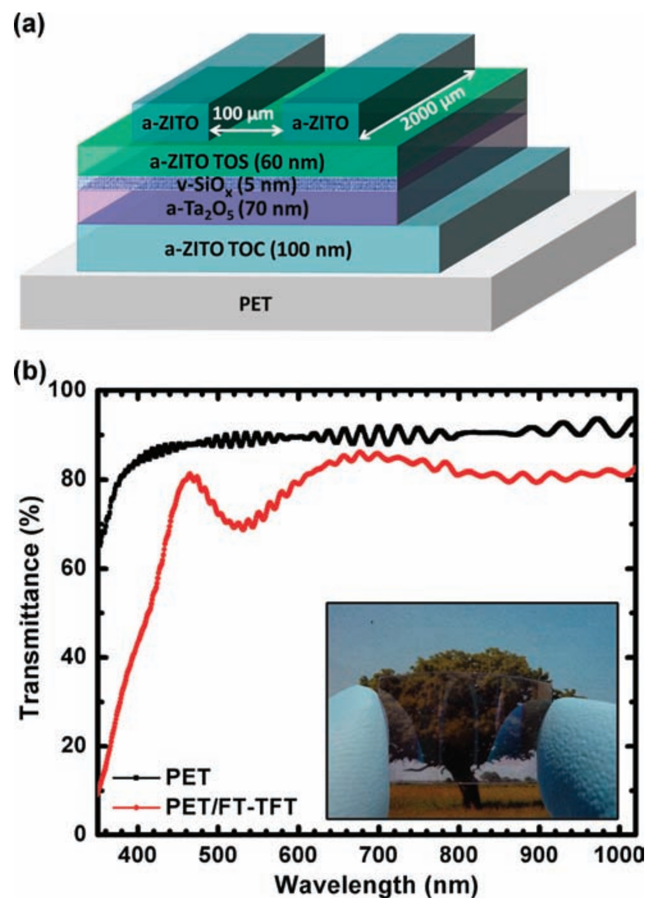

Figure 8. Structure of the present PET/a-ZITO TOC/(a-Ta_2O_5/v-SiO_x) TOI/a-ZITO TOS/a-ZITO TOC TF-TFTs (a) and optical transmission spectrum of an 80 TF-TFT array taken through the a-ZITO TOC source−drain region (b), with the inset showing a photograph of the all-amorphous-oxide TF-TFT array fabricated on PET, bent with fingers over a printed tree picture. The image was taken by a Panasonic DMC-ZS1 Lumix digital camera with no further color adjustment.

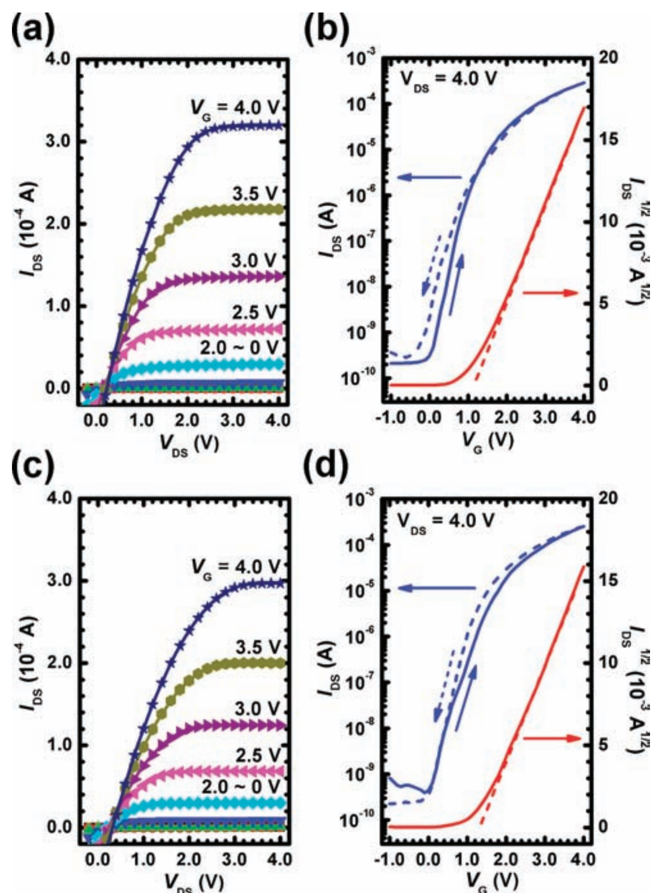

Figure 9. Representative output (a,c) and transfer (b,d) characteristics of identical TF-TFTs tested before (a,b) and after (c,d) repetitively bending 20 times along a curvature parallel to the channel length at a radius of 8 mm.

are rare. While a-ZITO TOS and TOC films can be grown at room temperature[8] and can serve as the TFT channel and electrodes, respectively, the a-Ta_2O_5/v-SiO_x bilayer TOI films reported here, with high C_i, low gate leakage, and enhanced interfacial compatibility with a-ZITO TOS channels, are also amorphous and provide exceptionally effective gate dielectrics in TFTs using p^+-Si gate and Au source−drain electrodes, as shown above. By next replacing the TFT electrodes with a-ZITO TOC materials, all-amorphous-oxide TF-TFTs having the structure shown in Figure 8a could be fabricated on PET substrates. Figure 8b shows the optical transmission spectrum of an 80 TF-TFT array acquired through the a-ZITO TOC source−drain region. The average visible transmittance of the TF-TFT array is ~75%. Note that the average visible transmittance of the PET substrate alone is ~90%. The photographic image (Figure 8b inset) also demonstrates the transparency and flexibility of these devices.

The output and transfer characteristics of these all-amorphous-oxide TF-TFTs are shown in Figure 9a,b. The results indicate that these TF-TFTs have n-type channels operating in the enhancement mode with the accumulation of electrons at positive gate biases. The output characteristics exhibit a steep I_{DS} rise with V_{DS} in the low V_{DS} region, suggesting good Ohmic contact properties between the a-ZITO TOC source−drain electrodes and the a-ZITO TOS channel. I_{DS} reaches saturation at $V_{DS} > 2.0$ V, and $I_{on} > 0.3$ mA is achieved at $V_G = 4.0$ V. Hysteresis in these TF-TFTs is almost negligible, but with a slightly negative V_T shift of ~0.1 V. The μ_{FE}, I_{off}, I_{on}:I_{off}, V_T, and SS values extracted from the transfer plot at $V_{DS} = 4.0$ V are ~20 $cm^2/V \cdot s$, ~10^{-10} A, >10^5, ~1.2 V, and ~0.26 V/decade, respectively (Table 1). Note that such low operating voltages, low I_{off}, and high I_{on}:I_{off} characteristics are very important to realizing the low power consumption needed for battery-powered portable electronics applications.

To assess the mechanical flexibility of the present devices, identical TF-TFTs were tested before and after repetitive bending 20 times along a curvature parallel to the channel length at a bending radius of 8 mm; the results are shown in Figure 9c,d. Note that the devices maintain excellent functionality with no serious degradation after bending, demonstrating the attraction of using all-amorphous-oxide components. The low I_{off} (<10^{-9} A) and high I_{on}:I_{off} (>10^5) parameters are nearly unchanged after bending, and the measured μ_{FE} is ~18 $cm^2/V \cdot s$, with $I_{on} \approx 0.3$ mA at $V_G = 4.0$ V, all comparable to the device performance parameters before bending.

Conclusions

In summary, a-Ta_2O_5 transparent oxide insulating films with a high κ of ~22.1 and an E_g of ~4.05 eV were grown by IAD at room temperature. Next, a-Ta_2O_5/v-SiO_x bilayer TOI dielectrics were fabricated by capping the IAD-derived a-Ta_2O_5 with a thin v-SiO_x layer, deposited by post-cross-linking a vapor-deposited $Cl_3SiOSiCl_3$-derived film. The resulting bilayer amorphous TOI dielectrics heterogeneously integrate the large

C_i from the high-κ a-Ta_2O_5 layer with the v-SiO_x layer, exhibiting improved TFT interfacial compatibility with an a-ZITO TOS channel layer over that of a-Ta_2O_5-only gate dielectrics. Transparent, flexible TFTs comprised exclusively of amorphous oxides are fabricated at low temperatures on PET substrates by combining the a-Ta_2O_5/v-SiO_x bilayer amorphous TOI gate dielectric with an a-ZITO TOS channel and a-ZITO TOC electrodes. These all-amorphous-oxide TF-TFTs exhibit excellent performance parameters of $\mu_{FE} \approx 20$ cm^2/V·s, $I_{on} > 10^{-4}$ A, and I_{on}:$I_{off} > 10^5$ at low operating voltages of ~4.0 V, along with good visible transparency and excellent mechanical flexibility, thereby offering a promising approach toward flexible "invisible" electronics.

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Supporting Information Available: MIS gate leakage current density at different gate voltage steps and time delays; transistor gate leakage data. This material is available free of charge via the Internet at http://pubs.acs.org.

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